### **TOPICAL REVIEW**

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### **Topical Review**

# Field-effect transistors engineered via solution-based layer-by-layer nanoarchitectonics

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#### Abstract

The layer-by-layer (LbL) technique has been proven to be one of the most versatile approaches in order to fabricate functional nanofilms. The use of simple and inexpensive procedures as well as the possibility to incorporate a very wide range of materials through different interactions have driven its application in a wide range of fields. On the other hand, field-effect transistors (FETs) are certainly among the most important elements in electronics. The ability to modulate the flowing current between a source and a drain electrode via the voltage applied to the gate electrode endow these devices to switch or amplify electronic signals, being vital in all of our everyday electronic devices. In this topical review, we highlight different research efforts to engineer field-effect transistors using the LbL assembly approach. We firstly discuss on the engineering of the channel material of transistors via the LbL technique. Next, the deposition of dielectric materials through this approach is reviewed, allowing the development of highperformance electronic components. Finally, the application of the LbL approach to fabricate FETs-based biosensing devices is also discussed, as well as the improvement of the transistor's interfacial sensitivity by the engineering of the semiconductor with polyelectrolyte multilayers.

Keywords: layer-by-layer assembly, field-effect transistors, nanoelectronics, nanoarchitectonics, nanomanufacturing

(Some figures may appear in colour only in the online journal)

#### 1. Introduction

Although it is commonly recognized that nanotechnology has a significant impact on the creation of materials that have nano-sized structures, it also provides notable benefits in the development of fabrication techniques to create advanced devices. These benefits include gaining a deeper comprehension of new phenomena in the nanoscale domain and the underlying physical principles that guide them [1-3]. Nonnanotechnology disciplines including supramolecular chemistry with self-assembly/self-organization [4-7], material fabrications [8-10], and biotechnology [11-13] are crucial to the development of functional materials from nanoscale units. As a result, the creation of materials from nanometric units in the nanoscale regime requires the application of a novel concept that combines nanotechnology ideas with the

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aforementioned different research fields. The resulting concept is known as 'nanoarchitectonics' [14–21].

Constructing functional architectures in three dimensions can be a complex task. In this regard, layer-by-layer (LbL) nanoarchitectonics involving various components offers a practical approach to showcasing the potential of nanoarchitectonics through the creation of functional materials and devices in which directional and dimensional aspects are considered.

Along the years a number of techniques have been created to precisely place specific materials in predetermined locations. However, achieving spatial nano-organization in complex systems through simple, reliable and affordable protocols is not a simple task. Therefore, in order to create nanoarchitected materials or nanoscale devices, it is essential to use an additive manufacturing process that has high spatial resolution [22], or a *nanoadditive manufacturing strategy* that allows for precise control over the deposition of different components [23, 24].

The production of modern electronic devices utilizing additive manufacturing methods illustrates the challenge of fabricating functional nanoscale films, which are crucial components in nearly all electronic devices. Let us take, for instance, thin-film field-effect transistors (FETs) that require precise assembly of conductors, semiconductors, and insulators as source/drain/gate electrodes, channels, and dielectrics, respectively, each with thicknesses on the order of tens of nanometers [25]. Field-effect transistors are critical building blocks in modern electronics, as they regulate the flow of current between a source and drain electrode through a semiconducting channel, which is controlled by the voltage applied to the gate electrode. Typically, a dielectric layer separates the semiconductor channel from the gate electrode. The type of charge carriers, either holes or electrons, in the semiconductor channel depends on its doping, resulting in different categories of FETs: p-type, n-type, or ambipolar [26]. As a result, the conditions in which different functional nanomaterials are integrated in thin film configurations into the FETs strongly affect the performance of the resulting device.

Control over thin film growth can be quite challenging using conventional additive manufacturing techniques [27, 28]. In this context, exploiting molecular forces, such as electrostatic interactions, can be a strategy for achieving self-regulated assembly of molecules, polymers, and/or nanomaterials into monolayers or sub-monolayers, enabling better control over film growth. This forms the foundation of a nanoadditive manufacturing technique [22] called 'layer-bylayer assembly' (LbL assembly), where a monolayer of a desired material is formed and then followed by the deposition of a second monolayer onto the first one. By repeating and cycling these steps, films with precise thickness and composition can be fabricated, allowing for controlled and customizable thin film manufacturing.

In this sense, LbL technique has demonstrated to be one of the most versatile approaches to grow functional nanofilms by the subsequent assembly of complementary materials. LbL assemblies exhibits the distinctive features of simplicity and inexpensive procedures [29, 30], as different multilayers can be constructed on a solid substrate by simply dipping the substrate into solutions of the desired components. On a laboratory scale, the fabrication processes can be accomplished simply with beakers and tweezers, employing adsorption steps of approximately 10 min. However, the technical implementation of this method is not limited to hand-processed dipping as the use of automated machines for LbL assembly [31] and spray-coating [32] have also been demonstrated. Electrostatic interactions have been widely exploited as the driving force in LbL assembly; however, this strategy has been extended to other interactions, such as hydrogen-bonding interactions [33], biospecific interactions [34], metal coordination [35], charge transfer [36], supramolecular inclusion [37], and sol/gel reactions [38]. In this regard, it should also be mentioned that achieving thicker films through the LbL assembly technique can be timeconsuming and challenging and-depending on the nature of the building blocks - the process can result in films with uneven surface roughness. However, researchers are actively working to address these limitations through various strategies, using different deposition techniques, or exploring new materials. These efforts aim to improve the dimensional stability, control over film structure, and expand the applicability of LbL assembly for diverse applications.

Compared to other fabrication techniques used for thin films, LbL assembly offers a significant level of versatility in terms of component applicability and technical feasibility. For instance, LbL assembly has been applied to a huge variety of target materials, including simple and functional polymers [39–50], macromolecular complexes [51–55], microgels [56], polymersomes [57], surfactant-based mesostructures [58–62], inorganic nanostructures [63, 64], and bioactive elements [65, 66], among other building blocks.

This kind of additive manufacturing method, which uses nanoscale thickness control in the ultrathin regime, has been very useful for creating and engineering the characteristics of FETs (figure 1). In the particular case of 2D material-based FETs, the implementation of optimized synthesis/exfoliation methods and separation/purification protocols also plays a critical role in the fabrication of uniform thin films and reliable devices [67].

In this topical review, we highlight research efforts to engineer field-effect transistors using the LbL assembly approach. We discuss different examples that illustrate the nanoarchitectonics concept. For FET fabrication, different LbL approaches were selected in order to show how the type of self-assembled nanomaterial can define the nature of the conduction of the semiconducting channel. Next, we discuss strategies for dielectric deposition via LbL. For the application of FETs as biosensing devices [26] we have selected examples in which enzymes act a biorecognition elements embedded in LbL assemblies since enzymatic nanobiosensors display high selectivity and affinity toward designated target molecules. Finally, we discuss on the use of the LbL strategy to improve the interfacial sensitivity by the engineering of the semiconductor with polyelectrolyte multilayers. We hope that the readers can find many inspirations for the development of construction of FET devices via solution-based LbL nanoarchitectonics from the presented examples.



Figure 1. Outline of nanoarchitectonics methodology to engineer field-effect transistors.

#### 2. Active channel material engineering via LbL

The channel material of FETs is one of the most relevant components of these type of electronic devices. Therefore, we firstly discuss on recent reports employing the LbL approach to engineer the channel material.

### 2.1. LbL assembly of carbon nanotubes for field-effect transistors

Single-walled carbon nanotubes (SWNTs) have garnered considerable interest as potential building blocks for electronic devices. For instance, by utilizing semiconducting SWNTs as the channel material, field-effect transistors (FETs) with impressive electrical properties have been developed. Typically, SWNT FETs exhibit p-channel characteristics, with holes as the dominant charge carriers, under ambient conditions [68]. In this regard, Duan et al [69] reported the construction of p-channel and n-channel single-walled carbon nanotube (SWNT) film-effect transistors (FETs) using a LbL assembly approach. The authors demonstrated that the utilization of polyethylenimine (PEI), known for its high electron-donating ability, enables the conversion of p-channel FETs to n-channel devices. Notably, the resulting n-channel devices exhibit air-stability even in environments outside of vacuum or inert conditions. To facilitate the uniform deposition of negatively charged SWNTs on the substrate, the device was pre-modified with LbL assemblies of poly (dimethyldiallylammonium chloride) (PDDA) and poly (sodium 4-styrenesulfonate) (PSS). This polyelectrolyte multilayer acted as an electrostatic 'glue'. Initially, the wafer was treated with PDDA to introduce positive charges on its surface, followed by a bilayer of PSS and PDDA to further enhance the surface charge density (figure 2(a)). Subsequently, the device was exposed to a SWNT solution for 30 min, resulting in the formation of a random-network SWNT film (figure 2(b)).

These devices exhibited p-channel characteristics (figure 2(c)) displaying an on/off current ratio (defined as the high current ( $I_{on}$ ) over the low current ( $I_{off}$ ) at a drain voltage of -5 V) of ~36.5. After the fabrication of p-channel devices, the assembly of a PEI layer on the random-network SWNT film converts the device to a n-channel (figure 2(d)). The presence of amine groups in PEI confers a high electron-donating ability, resulting in hole-depletion in p-channel SWNTs and the subsequent conversion to n-channel behavior. Moreover, the PEI coating on the devices serves to protect the SWNTs from exposure to air, mitigating the adverse effects of p-doping caused by O<sub>2</sub> adsorption.

The LbL strategy has been also employed to create SWNT FET devices based on nanocomposite multilayers. SWNTs and SiO<sub>2</sub> nanoparticles were assembled on a substrate as the semiconducting and dielectric materials, respectively [70]. In this configuration the respective layers were deposited on the substrate using polyelectrolytes as the intermediate adhesion components. The resulting devices were constituted of Si/SiO2 wafers with self-assembled SWNTs as the semiconducting material, SiO<sub>2</sub> nanoparticles as the gate dielectric material. Au as the source and drain electrode material, and Al as the gate electrode material (figure 3(a)). It is worth noting that the use of SiO<sub>2</sub> nanoparticles as dielectric materials has also been employed by Lvov and co-workers for the LbL construction of metal-oxide-semiconductor field-effect transistors (MOSFETs) [71]. One important aspect of the LbL construction strategy relies on the fact that the nanotube interconnection can be controlled by the number of assembled layers, with a concomitant effect on the conductivity and the carrier mobility of the thin-film transistors.

Experimental results for a set of SWNT devices with channel dimensions of  $W = 500 \ \mu m$  and  $L = 25 \ \mu m$  revealed a steep mobility increase as the number of assembled layers (*n*) increased from 1 to 3. In this range, the mobility is increased ~35 times. Then, upon increasing the number of



**Figure 2.** (a) Structure of the carbon nanotube thin-film transistor. (b) SEM image of random-network SWNTs on top of a PDDA + PSS bilayer between the source and drain electrodes. Output characteristics of (c) a p-channel FET and (d) an n-channel FET based on self-assembled random SWNTs networks. Reprinted from [69], Copyright (2013), with permission from Elsevier.



**Figure 3.** (a) The structure of the carbon nanotube thin-film transistor (TFT) is shown, with an enlarged view of the LbL self-assembled carbon nanotube semiconducting layer and SiO<sub>2</sub> nanoparticle dielectric layer. (b) The mobility of SWNT TFTs with different numbers of SWNT layers (*n*: 1–7) is depicted in the main panel for devices with a width (*W*) of 500  $\mu$ m and a length (*L*) of 25  $\mu$ m. The inset shows the mobility versus *n* for devices with  $W = 500 \,\mu$ m and  $L = 50 \,\mu$ m. Reprinted from [70], Copyright (2009), with permission from Elsevier.

layers a slight decrease in mobility is observed (figure 3(b)). A similar trend is observed in another set of transistor with different design parameter ( $W = 500 \,\mu\text{m}$  and  $L = 50 \,\mu\text{m}$ ) (figure 3(b) inset). The mobility greatly increases first, and slowly decreases to a smaller value afterwards. Experiments show that the highest observed mobility is ~333 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup>. The variation in mobility with the number of assembled

SWNT layers can be attributed to the interconnections formed among the SWNTs. SWNTs from different layers can penetrate through the polyelectrolyte layers and establish connections with each other. These interconnections increase the effective thickness of the semiconducting film and enhance the mobility of the conductive channel. A similar approach to fabricate high-mobility thin-film transistors (TFTs) using LbL-assembled SWCNTs (as the semiconducting material) and SiO<sub>2</sub> nanoparticles (as the gate dielectric material) was reported by Xue *et al* [72]. In this approach, LbL-assembled SWCNT devices exhibited *p*-type semiconductor characteristics with a hole mobility ( $\mu$ p) of 168.5 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup>, and an on/off current ratio ( $I_{on/off}$ ) of 4.2. In this context, we should also mention that SWCNT FETs prepared by direct adsorption in which the network density is adjusted by the adsorption time or the SWCNT concentration also exhibit remarkable performance [25].

#### 2.2. LbL assembly of graphene for field-effect transistors

Graphene has been a subject of intense research and development due to its remarkable electronic properties, such as high intrinsic carrier mobility and ambipolar behavior, as well as excellent chemical and mechanical stability and high thermal conductivity. These properties make graphene a promising material for nanoelectronics, particularly in fieldeffect transistor (FET) applications. To fabricate graphenebased transistors, low-cost and reliable methods for depositing graphene onto various substrates have been sought after. Within this framework, solution processes have emerged as versatile strategies for engineering graphene devices. Solution-based methods offer advantages such as scalability, costeffectiveness, and compatibility with various substrates, including flexible substrates. These methods typically involve the dispersion of graphene in a liquid solution, followed by deposition onto a substrate through techniques such as spin coating, drop casting, inkjet printing, or spray coating. Solution processes allow for precise control over graphene film thickness, coverage, and morphology, which can be critical for optimizing device performance.

Solution-based methods have been widely explored for graphene deposition due to their flexibility and potential for large-scale production. These methods have enabled the fabrication of graphene FETs with various device architectures, including top-gate and bottom-gate configurations, and have been utilized in diverse applications ranging from flexible electronics to biosensors. However, challenges still exist in terms of achieving uniform and high-quality graphene films with controlled electrical properties across large areas, and ongoing research is focused on further refining solutionbased methods for graphene device fabrication. In this context, Hwang et al [73] proposed a systematic method to tune the characteristics of graphene field-effect transistors by using the LbL assembly of positively and negatively charged graphene oxide nanosheets followed by thermal or chemical reduction (figure 4).

Suspensions of graphene oxide (GO<sup>-</sup>) that carry a negative charge, prepared using the Hummers method, were assembled sequentially with suspensions of positively charged graphene oxide (GO<sup>+</sup>). The GO<sup>+</sup> suspensions were modified with  $NH_2$  groups on the graphene oxide nanosheets.

An interesting characteristic of this graphene interfacial architecture is that the ambipolar or unipolar (both n-type and p-type) transport of the transistors is dependent on the number of self-assembled layers, as illustrated in figure 5. In figure 5(a), the plots of conductance (G) versus gate voltage (V<sub>G</sub>) for transistors made from thermally reduced graphene oxide (TRGO) multilayer films with varying numbers of graphene oxide bilayers are shown. The results reveal that the charge transport properties of TRGO field-effect transistors (FETs) are significantly influenced by the number of assembled layers, with a corresponding increase in film conductance as depicted in figure 5(b). Experimental findings indicate that TRGO FETs assembled using the LbL method with two bilayers exhibit unipolar p-type conduction, which is different from the typical ambipolar transport observed in graphene FETs [74].

On the other hand, as the number of bilayers is increased, the influence of the SiO<sub>2</sub> substrate is reduced and Dirac voltage is shifted toward more negative voltage values (figure 5(c)). This implies that the electron doping increases with the number of assembled bilayers. As a result, the symmetric ambipolar transport displayed by graphene transistors is observed in five-bilayered TRGO FETs. Further characterization of these devices revealed that six-bilayered TRGO films exhibit a unipolar n-type conduction. It is worth noting that these significant changes in transport properties, transitioning from almost p-type to ambipolar and then to n-type transport, occur within a mere difference of four bilayers in TRGO films. In contrast, similar experiments conducted on transistors made from chemically reduced graphene oxide (CRGO) multilayer films showed no significant alterations in the transport type or a shift in the Dirac voltage with varying numbers of assembled layers. This suggests that the post-assembly treatment, such as chemical reduction or thermal treatment, plays a crucial role in determining the electron transport characteristics of multilayer graphene films.

Along these lines, Müllen and co-workers [75] proposed an interesting twist to the creation of graphene transistors through solution-based LbL techniques. In their approach, graphene oxide (GO) nanosheets and Keggin-type polyoxometalate clusters H<sub>3</sub>PW<sub>12</sub>O<sub>40</sub> (PW), were co-assembled into multilayer films via electrostatic LbL assembly (figure 6(a)). The assembly process is regulated by electrostatic interactions between the negatively charged surface of graphene oxide (GO) nanosheets and polyoxometalate (PW) clusters, in combination with cationic polyelectrolytes such as PEI and polyallylamine hydrochloride (PAH). Initially, the substrates are modified by depositing a PEI/PW double layer as precursor films. Subsequently, varying numbers of PAH/GO/PAH/PW layers are deposited on these modified substrates to construct multilayer films consisting of GO nanosheets and PW clusters linked by PAH layers (figure 6(a)).

The central paradigm of this approach relies on the photocatalytic activity of PW clusters under UV irradiation, in which a photoreduction reaction takes place within the film resulting in the conversion GO in reduced GO (rGO). By this strategy, uniform and large-area composite films based on rGO can be prepared with precisely controlled thickness on various substrates. In this scenario, the LbL assembly favors the effective interaction between oxygen-containing groups on GO nanosheets and PW clusters, which is beneficial for the electron transfer from photoexcited PW to GO, thus realizing an efficient reduction process.



Figure 4. A diagram illustrating the LbL assembly of field-effect transistors (FETs) using graphene-based materials. Reprinted with permission from [73]. Copyright (2012) American Chemical Society.



**Figure 5.** (a) transfer characteristics of field-effect transistors (FETs) based on thermally reduced graphene oxide (TRGO) with different numbers of graphene oxide bilayers (b) The relationship between the number of bilayers in graphene oxide and the minimum conductance of TRGO FETs. (c) Variations in Dirac voltage observed in FETs based on TRGO (thermally reduced graphene oxide) and CRGO (chemically reduced graphene oxide) as the number of graphene oxide bilayers changes. Reprinted with permission from [73]. Copyright (2012) American Chemical Society.

FET devices were fabricated to assess the transport performance of the graphene films. These devices were fabricated using  $(PAH/GO/PAH/PW)_1$  and  $(PAH/GO/PAH/PW)_6$  films as starting materials. The electron and hole

mobilities were determined by analyzing the linear regime of the transfer characteristics of the FETs (figures 6(b), (c)).

From the  $I_{sd}$ - $V_g$  curves, hole and electron mobility values resulted in  $\mu_h = 0.03$  and  $\mu_e = 0.01 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  for the



**Figure 6.** (a) Scheme illustrating the fabrication process for reduced graphene oxide (rGO)-polyoxometalate (PW) multilayer films using a layer-by-layer (LbL) assembly approach. The process involves the sequential deposition of GO nanosheets and PW clusters using cationic polyelectrolytes, polyethylenimine (PEI), and polyallylamine hydrochloride (PAH), which act as electrostatic linkers. Subsequently, an in situ photoreduction step is carried out to convert GO to rGO,  $I_{ds}-V_g$  curves of the FET devices fabricated on a (PAH/GO/PAH/PW)<sub>1</sub> film (b) and a (PAH/GO/PAH/PW)<sub>6</sub> film (c). Reprinted with permission from [75]. Copyright (2011) American Chemical Society.

 $(PAH/GO/PAH/PW)_1$  film device, and  $\mu_h = 0.15$  and  $\mu_e = 0.06 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  for the  $(PAH/GO/PAH/PW)_6$  film device. It has been reported that the presence of water and oxygen on rGO FET devices might result in hole-dominated transport [76, 77]. The assemblies of  $(PAH/GO/PAH/PW)_n$  structures exhibit hole-dominated transport characteristics in FET devices due to the cage-type structure of PW that can trap electrons [78]. The on/off ratio, which is the ratio of maximum and minimum values of source-drain current ( $I_{sd}$ ), for  $(PAH/GO/PAH/PW)_1$ - and  $(PAH/GO/PAH/PW)_6$ -based devices is approximately 2.0 and 1.1, respectively. These values are similar to those reported for rGO films prepared by chemical or thermal reduction methods [79]. Moreover, devices fabricated with thicker films show higher mobility and lower on/off ratio. The precise control over the number of layers deposited on the substrate, which is one of

the advantages of LbL assembly, allows for the fabrication of rGO-based FET devices with high quality, uniformity, and tailorable properties. This nanoarchitectonics approach offers a simple and efficient method for fabricating rGO-based FET devices with desired characteristics.

Regarding the fabrication of graphene field-effect transistors using LbL assembly of oppositely charged reduced graphene oxide (rGO) nanosheets, Zucolotto and coworkers [80] demonstrated that highly conductive films can be formed by assembling reduced graphene oxide (rGO) multilayers on interdigitated gold electrodes. The conductivity of these films can be controlled by the number of deposited layers, with thermal annealing at 150 °C significantly increasing the conductivity. When these films were used in solution-gated field-effect transistors, they exhibited high transconductance values for both holes and electrons: 90  $\mu$ S and 55  $\mu$ S for holes



**Figure 7.** Transfer curves of papain-functionalized (rGO-SiNH<sub>2</sub>/ rGO-N) FETs in diluted synthetic urine in the presence of cystatin C at different concentrations. Reprinted from [80], Copyright (2021), with permission from Elsevier.

and electrons, respectively. These researchers further modified the graphene transistors with papain and were able to detect Cystatin C protein, a biomarker for chronic renal disease, in synthetic diluted urine at concentrations as low as  $5 \text{ ng ml}^{-1}$ . Dilution was necessary to overcome detection limitations due to variations in the Debye length near the transistor surface. The transfer curves of the graphene transistors in the presence of Cystatin C protein showed a decrease in current  $(I_{DS})$  and a shift to positive voltage values at the minimum conductivity point, indicating the potential of these graphene transistor devices as sensors and biosensor platforms. Figure 7 displays the transfer characteristics of graphene transistors assembled using the LbL technique, when exposed to Cystatin C protein. Under synthetic urine conditions at a pH of  $\sim$ 6.4, the papain-cystatin C complex exhibits a positive charge. This alteration in the electrostatic environment surrounding the FET device leads to a decrease in  $I_{DS}$  (source-drain current) with increasing cystatin C concentration, and a positive shift in the voltage at the minimum conductivity point. These findings highlight the potential of LbL-assembled graphene FET devices for use as sensors and biosensor platforms.

#### 2.3. FETs based on multilayered graphene oxide and PEDOT:PSS

LbL assembly presents a promising approach for creating composite graphitic materials with electrical anisotropy, achieved through simple and affordable experimental protocols. A recent study by Gomes *et al* [81] reported the fabrication of a self-assembled multilayer composite based on graphene, exhibiting remarkably high electrical anisotropy,

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with in-plane conductivity measuring five orders of magnitude higher than cross-plane conductivity. This unique property of LbL-assembled materials opens up possibilities for utilizing them as semi-insulators for cross-plane conduction and semiconductors for in-plane conduction. Notably, this interfacial architecture of LbL-assembled materials lacks a distinct boundary between insulator and semiconductor layers, which typically leads to the formation of interfacial defects known to adversely affect device performance by acting as charge-carrier traps or scattering centers [82, 83]. In this particular case, the transistor architecture was fabricated by stacking multilayers of graphene oxide (rGO) and poly(3,4-ethylenedioxythiophene):polystyrenesulfonate (PEDOT:PSS) embedded in a polymeric matrix composed of polyethylenimine (PEI) and poly(acrylic acid) (PAA) onto interdigitated electrodes (IDE).

The LbL films were created through assembly of PEI and nanoplatelets of reduced graphene oxide (rGO) functionalized with PAH (GPAH) as cationic building blocks and an anionic solution consisting of PAA, rGO functionalized with poly(styrene-sodium sulfonate) (GPSS), and poly(3,4-ethylenedioxythiophene):polystyrene sulfonate (PEDOT:PSS) (figures 8(a), (b)).

Devices were manufactured by depositing 30 bilayers of (PEI + GPAH/PAA + GPSS + PEDOT:PSS) on planar gold interdigitated electrodes (IDEs) (figure 8(c)). The currentvoltage characteristics of the fabricated devices were measured under low applied voltages ( $V_{ds} < 1$  V) and are illustrated in figure 8(d). Notably, the drain-source current  $(I_{ds})$  does not reach the saturation regime as commonly observed in conventional transistor output curves. A gate voltage of only 0.65 V results in a 20  $\mu$ A increase in channel current, corresponding to an  $I_{ds}$  modulation of 27%. Furthermore, the  $I_{ds}$  increases with positive gate voltage, indicating an n-type channel field-effect transistor (FET) behavior. Previous work has shown that the GPAH/GPSS structure exhibits preferred n-type conduction [84], suggesting that the dominant transport mechanism in this type of nanocomposite transistor occurs through the rGO-aligned layers. However, the performance of the transistor is limited by the high background current, which hinders optimal channel modulation. Nevertheless, this limitation can be addressed by optimizing the multilayer assembly process and functionalization of the building blocks.

## 2.4. LbL-assembled two dimensional semiconductors as active channel materials in FETs

In the last decade there has been an explosion of interest in the use of two-dimensional materials from layered semiconductors in electronics and optoelectronics applications [85–87]. Despite the promising horizons of this scientific area, one critical aspect that precludes the practical involvement of 2D materials—such as transition-metal dichalcogenides (TMDs)—in electronics industry is the production of wafer-scale thin films. Although chemical vapor deposition has been utilized to produce high-quality monolayer transition metal dichalcogenides (TMDs), their



**Figure 8.** Chemical structures of cationic (a) and anionic (b) building blocks LbL-assembled in a multilayer structure. (c) Schematic representation of the device showing the underlying interdigitated electrode (IDE) and the active layer consisting of 30 bilayers of (PEI + GPAH/PAA + GPSS + PEDOT:PSS) assemblies. (d) Current–voltage characteristics of the as-fabricated FET device. The top inset shows the transfer curve measured in the linear region with |Vds| = 0.35 V, and the leakage current (*I*gs). The inset on the bottom depicts the electrical connections of the device. [81] John Wiley & Sons. [© 2021 Wiley-VCH GmbH].

application in flexible and large-area represents a difficult task due to the demanding operational conditions and laborious transferring procedures to different substrates [88-90]. As an alternative approach, the scientific community has been investigating the assembly of uniform thin films from dispersions of 2D flakes exfoliated from bulk crystals. Colloidal inks of MoS<sub>2</sub> and WS<sub>2</sub> have been used as starting materials for the construction of active channels for fieldeffect transistors via inkjet or spray printing [91-93]; however, the performance of these as-synthesized devices is inferior to CVD-grown thin films due to the poor quality of solution-processed 2D flakes [94]. It has been demonstrated that spin-coating of MoS<sub>2</sub> nanosheets produced via electrochemical exfoliation leads to devices with improved characteristics [95]. However, the spin-coating-based fabrication method also leads to microscale accumulation of nanosheets resulting from drying effects. In this context Gao et al [96] showed that LbL assembly represents a versatile strategy for fabricating semiconducting thin films from 2D materials. Contrary to spin-coating, the self-limiting nature of LbL assembly offers the chance to put into practice an additive nanomanufacturing technique capable of producing composite multilayers with precise control over film thickness. By simply using a polyelectrolyte - such as PDDA -as an 'electrostatic glue', electrochemically exfoliated MoS<sub>2</sub> dispersions can be used to FET channels on any selected substrate. Moreover, in LbL assembly, planar surfaces are not necessary for the full implementation of the fabrication technique, thus allowing for patterning through a straightforward lift-off process instead of a costly reactive ion etching (RIE) technique.

Semiconducting films were prepared by alternately immersing substrates into PDDA solutions (cationic building blocks) and MoS<sub>2</sub> dispersions (anionic building blocks), leading to a layered deposition of polyelectrolytes and MoS<sub>2</sub> nanosheets (figure 9(a)). The sequential LbL process after *n* cycles leads to (PDDA/MoS<sub>2</sub>)*n* films wherein the loading of MoS<sub>2</sub> in the films exhibits a linear dependence on the cycling number (*n*) (figure 9(b)).

One interesting aspect of these LbL-assembled architectures relies on the fact that the interfacial spacing is short enough to allow the electrons to tunnel through the contacting flakes. As a result, the LbL leads to a percolating MoS<sub>2</sub> network. In this way, ion gel gated FET devices were fabricated employing (PDDA/MoS<sub>2</sub>)<sub>1</sub> thin films which are treated by immersing in bis(trifluoromethane) sulfonimide (TFSI) for 2 h with subsequent thermal treatment at 300 °C. Figure 9(c) shows a typical n-type  $I_{sd}$ - $V_g$  transfer character-istics with on/off ratios of  $1.1 \times 10^5$  when  $V_{sd} = 0.1$  V and  $V_{\rm g}$  varies between -2 and 2 V. In this preparative strategy, the chemical and thermal processing of the LbL assembled films is necessary to improve the charge transport properties of the device. The corresponding  $I_{sd}-V_{sd}$  output characteristics of these FETs (channel length:  $L = 5 \,\mu m$ , channel width:  $W = 100 \,\mu\text{m}$ ) display a linear trend at small  $V_{sd}$  and gradually saturates at larger  $V_{sd}$  (figure 9(d)).

Maximum on-currents obtained from these devices can reach 700  $\mu$ A - or 7  $\mu$ A  $\mu$ m<sup>-1</sup> after normalization - when  $V_{sd} = 1$  V and  $V_g = 2$  V. It is worth noting that the performance of these FETs fabricated through LbL assembly exceeds that of other solution-processed TMD FETs reported in the literature (with current values ranging from 0.08 to 0.3  $\mu$ A  $\mu$ m<sup>-1</sup>) [97, 98], and is comparable to devices



**Figure 9.** (a) Schematic representation of the fabrication process of  $MoS_2$  thin films through a LbL assembly strategy. (b) Representation of the thickness of  $(PDDA/MoS_2)_n$  thin films as a function of the number of bilayers. (d)  $I_{sd}-V_g$  transfer characteristics of the FETs gated by ion gels at  $V_{sd} = 0.1$  V. (e)  $I_{sd}-V_{sd}$  output characteristics of the same FET in (d). (f) Comparison of mobilities and on/off ratios ( $log(I_{on}/I_{off})$ ) for  $MoS_2$  FETs prepared by different methods. Reproduced from [96], with permission from Springer Nature.

fabricated from CVD or mechanically exfoliated TMDs (with current values ranging from 0.1 to 13  $\mu$ A  $\mu$ m<sup>-1</sup>) [99, 100]. Furthermore, the electron mobility of these FETs reaches 4.7 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup>, thus surpassing the typical values reported for solution-processed TMD FETs fabricated via spin-coated or inkjet-printed thin films (as shown in figure 9(e)). In<sub>2</sub>Se<sub>3</sub> thin films with uniformity have been successfully created using a similar approach through LbL assembly of PDDA and electrochemically exfoliated In<sub>2</sub>Se<sub>3</sub> [101]. These LbL-assembled In<sub>2</sub>Se<sub>3</sub> thin films were employed as active channel materials in FETs and exhibited excellent device performance. Notably, the electron mobilities and on/off ratios of the LbL-assembled In<sub>2</sub>Se<sub>3</sub> thin films were comparable to those of spin-coated In<sub>2</sub>Se<sub>3</sub> thin films and chemical vapor deposition (CVD)-grown In<sub>2</sub>Se<sub>3</sub> thin films [102, 103].

These findings highlight the potential of LbL assembly as a viable technique for processing thin films from solutionprocessed semiconducting materials, offering scalability and cost-effectiveness for the fabrication of electronic devices.

#### 3. Deposition of dielectrics via LbL assembly

The advancement of methods and approaches for manipulating dielectric capacitive components has garnered significant attention in the realm of solution-processed nanoelectronics. The gate dielectrics plays a direct role in influencing key device parameters such as mobility, hysteresis, and power consumption in high-performance nanoelectronics. Notably, the areal capacitance, which is determined by the thickness and dielectric constant of the material, is crucial in tailoring device characteristics. For this reason, precise control of the thickness during thin film preparation is of paramount importance for obtaining optimized dielectric layers with large areal capacitance and low leakage current, which are essential for the operation of FETs at low voltages and power levels [104, 105].

#### 3.1. LbL assembly of ultrathin dielectrics for FET applications

In comparison with vacuum-based thin-film deposition processes, such as atomic layer deposition or chemical vapor deposition [106, 107], solution-based LbL assembly offers a more economical and scalable strategy to create tailored films. In fact, the LbL approach also offers advantages over spin coating (a conventional solution-based deposition method) in controlling thickness at the ultrathin limit [108, 109].

Hersam and workers [110] have introduced an effective technique for constructing scalable and ultra-thin dielectrics using 2D montmorillonite (MTM) nanosheets via a LbL assembly strategy. These authors demonstrated that this LbL approach resulted in the rapid formation of sub-10 nm thin films composed of 2D MTM nanosheets, exhibiting high capacitances of approximately 600 nF cm<sup>-2</sup> and low leakage currents as low as  $6 \times 10^{-9}$  A cm<sup>-2</sup>. The films were assembled on p-type doped Si substrates by immersing the substrate in cationic PEI solution and an aqueous dispersion of negatively charged exfoliated MTM nanosheets in a sequential manner. The deposited [PEI/MTM]<sub>n</sub> films, where *n* represents the number of cycles, exhibited high uniformity with complete coverage of the Si surface by overlapping MTM nanosheets after the LbL process. Importantly, the



**Figure 10.** (a) Scheme illustrating the metal–insulator–semiconductor structure employing montmorillonite (MTM) multilayers as dielectric materials. (b) J versus electric field for  $[PEI/MTM]_3$  after annealing at different temperatures. [110] John Wiley & Sons. [© 2015 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim].

adsorption time for the LbL assembly could be reduced to as little as 10 seconds, while maintaining the critical functional aspects of the films intact.

After assembly, thermal annealing was employed to eliminate the hygroscopic PEI from the  $[PEI/MTM]_n$  films, as it can cause high leakage currents due to absorbed water. Indeed, the thermal treatment presents a viable approach to integrate a robust dielectric film into FET devices through a solution-based process, as PEI decomposes at around 300 °C and disappears completely at 600 °C in air, while MTM remains stable at these elevated temperatures (figure 10(a)). Experimental data obtained from figure 10(b) suggests that the leakage current of [PEI/MTM]<sub>3</sub> films decreases as the annealing temperatures increase, indicating the gradual removal of the PEI component from the films. The film annealed at 300 °C shows high leakage and is not suitable as a gate dielectric. However, the film annealed at 400 °C demonstrates a lower leakage current density of 2.4  $\times ~10^{-5}\,A\,cm^{-2}$  at an applied electrical field of  $2 \,\mathrm{MV}\,\mathrm{cm}^{-1}$ , with values comparable to self-assembled organic dielectrics [111]. These values of leakage current densities can be further reduced to  $8 \times 10^{-8} \,\mathrm{A \, cm^{-2}}$  and  $6 \times 10^{-9} \,\mathrm{A \, cm^{-2}}$  with increasing annealing temperatures to 500 °C and 600 °C, respectively.

The LbL assembly of dielectric nanofilms exhibiting leakage currents, below  $10^{-8}$  A cm<sup>-2</sup> has enabled the operation of both p-type semiconducting SWCNT and n-type indium gallium zinc oxide (IGZO) FET devices at low voltages. These promising results highlight the potential of LbL-assembled MTM nanosheet dielectrics for solution-processed nanoelectronic applications.

A similar approach was employed by the same research group to fabricate hexagonal boron nitride (h-BN) thin films [112]. While high quality, atomically thin h-BN has been prepared via expensive, time-consuming and laborious chemical vapor deposition process [113], traditional liquid exfoliation methods offers scarce control over h-BN thickness and large-area film quality, thus limiting its use in solutionprocessed electronics.

In this way, the application of isopycnic density gradient ultracentrifugation as a method for the preparation of monodisperse, thickness-sorted h-BN dispersions has opened the door to the use of these 2D nanomaterials as high-quality building blocks for LbL assembly. Along these lines, Zhu *et al* demonstrated that the sequential assembly of PEI and h-BN dispersions leads to the construction of [PEI/ BN]<sub>n</sub> films with uniform, sub-10 nm thicknesses. After the film was assembled, a thermal annealing process was carried out at 600 °C to enhance the performance of the film and create a h-BN dielectric layer without any polymer content. As a result of the annealing process, the PEI component in the film underwent complete decomposition (figure 11(a)).

The resulting ultrathin dielectric layers showed excellent electrical properties, with low leakage currents of  $3 \times 10^{-9}$  A cm<sup>-2</sup> at an electric field of 2 MV cm<sup>-1</sup>, along with high capacitances of 245 nF cm<sup>-2</sup>. These favorable characteristics made it possible to fabricate graphene fieldeffect transistors using these dielectric layers (figure 11(b)) with negligible hysteresis and high mobilities up to 7100 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup> at room temperature. The transfer characteristics ( $I_d - V_g$ ) of the graphene transistors using a dielectric [h-BN]<sub>4</sub> layer reveals an approximately symmetric ambipolar behavior (figure 11(c)), thus indicating a minimal charge trapping in the h-BN dielectric. In a similar vein, the Dirac point ( $V_{\text{DIRAC}}$ ) is slightly negative with an average value of  $-0.14 \pm 0.05$  V, which implies negligible h-BN induced doping.

In comparison, graphene transistors employing  $SiO_2$  and  $HfO_x$  dielectric platforms show more significant hysteresis and possess highly positive  $V_{DIRAC}$ , thus suggesting that the LbL approach using h-BN inks contributes to minimizing the effects of underlying traps, resulting in improvements in overall device performance.



**Figure 11.** (a) Fabrication of h-BN dielectric thin film through LbL assembly. (b) Structure of the graphene field-effect transistor using LbLassembled h-BN thin films as dielectric materials. (c) Transfer curve of a GFET on an assembled h-BN ultrathin film showing negligible hysteresis. Reprinted with permission from [112]. Copyright (2015) American Chemical Society.

### 3.2. LbL assembled elastomeric dielectrics for FET applications

Elastomeric dielectrics have been recognized as critical components in the advancement of flexible/stretchable electronics due to their significant role in regulating carrier densities in semiconducting channels during deformation in soft/stretchable FETs. It is important to note that the dielectrics positioned between the gate electrode and the semiconducting channel are responsible for the electrostatics of FETs, and control the current flow between the source and drain electrodes [114]. Various approaches have utilized thick films as elastomeric dielectrics, which have impacted the operational conditions of FETs, such as increased voltage or power consumption for on/off operations [115, 116].

Recently, Zhu and co-workers [117] employed a LbL assembly approach to build 15 nm thick elastomeric nanodielectrics through sequential assembly of oppositely charged polyurethanes (PUs) (figures 12(a), (b)), thus leading to the fabrication of soft and hysteresis-free FETs.

Figure 12(c) depicts the change in film thickness during the assembly process. The trend observed is a consistent and almost linear increase in film thickness with the bilayer thickness. This trend may indicate that the film is growing uniformly and steadily with each additional bilayer, without any significant fluctuations or deviations from linearity. It was observed that the thickness decreases from 19.9 to 17.6, 15.4 and 13.6 nm when films are annealed at 140 °C, 170 °C and  $210 \,^{\circ}$ C, respectively (figure 12(c)). In line with this observation, the root-mean-square roughness (RMS) of the films is reduced after the annealing treatment (figure 12(d)). The implementation of a mild thermal annealing treatment after the assembly process facilitated the elimination of pinholes, thus resulting in PU multilayers exhibiting high areal capacitances of 237 nF cm<sup>-2</sup> and low leakage current densities of  $3.2 \times 10^{-8} \,\mathrm{A \, cm^{-2}}$  at 2 V.

PU nanodielectrics were also used in SWCNT FETs fabricated on rigid silicon or polyimide (PI) substrates, as shown in figure 13(a). Figures 13(b)–(c) illustrate typical

p-type transfer and output characteristics of the FETs, which were fabricated on an Al/Si substrate. PU nanodielectrics were further demonstrated in SWCNT FETs on rigid silicon or PI substrates (figure 13(a)). Figures 13(b)–(c) shows the p-type transfer and output characteristics of FETs fabricated on an Al/Si substrate. Upon applying a source-drain voltage ( $V_{\rm D}$ ) of -0.5 V, it is observed a modulation of the source-drain current ( $I_{\rm D}$ ) at low gate voltages ( $V_{\rm G}$ ) of -1.5 to 0 V with an on-current of 3.7  $\pm$  1.8  $\mu$ A, on/off ratio of 4.5  $\pm$  0.3  $\times$  10<sup>4</sup>.

The study found that the performance of the SWCNT FETs with PU nanodielectric films remained consistent even when fabricated on flexible PI (polyimide) substrates, as shown in figures 13(d)–(f). Even when the PI substrate was subjected to a bending strain of 5%, the maximum on-state currents and on/off ratios of the devices remained almost unchanged, indicating good stability under mechanical deformation. Furthermore, it was observed that the threshold voltages of the FETs were negatively shifted (i.e. reduced) with increasing bending strain, as shown in figure 13(f). Importantly, when the strain was relaxed and the PI substrate returned to a flat state, the performance of the SWCNT FETs recovered, indicating the ability of the PU nanodielectric film and the SWCNT network to withstand and adapt to mechanical deformation.

Due to the elastomeric nature of building blocks, even after being repeatedly stretched to a strain of 50%, the wrinkled counterparts exhibit remarkable mechanical stability, as evidenced by minimal changes in leakage currents, indicating their reliable electrical performance under mechanical stress. Noteworthy, the performance and overall characteristics of these films are not affected by high humidity environments and retain their properties upon immersion into water.

These results illustrate the versatility of the LbL approach to fabricate CTs-based FETs operating under low-voltage conditions with negligible hysteresis using nanodielectric films assembled from aqueous polyurethane-based building blocks.



**Figure 12.** (a) Chemical structures of charged polyurethanes (PUs). (b) Assembly process of PU nanodielectrics. (c) Thickness evolution with increasing number of cycles and thermal annealing. (d) Roughness of  $(PU^+/PU^-)_3$  nanofilms at different annealing temperatures. [117] John Wiley & Sons. [© 2021 Wiley-VCH GmbH].



**Figure 13.** (a) Optical image of SWCNT FETs with PU nanofilms as the dielectric on Al/Si substrate. (b) Transfer curves and (c) output curves of a SWCNT FET. (d) Schematic of a SWCNT FET on a flexible PI substrate. (e) Ion/Ion–flat and (f) Threshold voltages of the SWCNT FET at different strains. [117] John Wiley & Sons. [© 2021 Wiley-VCH GmbH].

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**Figure 14.** (a) A representation depicting the interdigitated channel of a solution-gated field-effect transistor (FET) utilizing reduced graphene oxide (rGO).b) Scanning electron microscopy (SEM) images showing an interdigitated channel that has been modified with reduced graphene oxide (rGO); scale bar = 100  $\mu$ m (top) and scale bar = 10  $\mu$ m (bottom) (c) Transfer characteristics of a field-effect transistor (FET) based on reduced graphene oxide (rGO) modified with sodium 1-pyrenesulfonate (SPS) via solution assembly. The experimental data were obtained at a fixed source-drain potential  $V_{ds}$  (0.1 V) in 10 mM KCl and 0.1 mm HEPES solution with pH varying from 5 to 10. An Ag/AgCl gate electrode was used for the measurements. (d) Illustration depicting the LbL deposition process. (e) Scheme of the urease-PEI multilayer film and the urease-catalyzed hydrolysis of urea. (f) Deprotonation of the PEI layer as a result of the catalytic activity of urease. Reprinted from [131], Copyright (2017), with permission from Elsevier.

# 4. Channel interface functionalization via LbL assembly

FETs play a pivotal role in signal transduction, showing exceptional capabilities for label-free, ultra-sensitive, and real-time detection [118]. In this regard, the detection of events happening at the interface of the channel is one of the most employed methods for the development of FET-based recognition devices [119, 120]. Therefore, the functionalization of the channel interface is a pre-requisite for an efficient interaction with the desired element and a specific detection.

## 4.1. Biosensors based on LbL-assembled polyelectrolyte multilayers on field-effect transistors

Biosensors with high selectivity are a potent tool for real-time measurement of diverse analytes with significant importance in areas such as food safety, environmental monitoring, drug screening, and diagnosis [121]. Enzymes are particularly advantageous as recognition elements due to their inherent specificity and selectivity towards the target analyte [122]. Leveraging the availability and biocompatibility of enzymes, their integration onto sensor surfaces presents an powerful approach for detecting specific substrates, while the versatility of enzymes, including enzymatic cascade reactions, makes this approach applicable to a wide spectrum of analytes [123, 124].

Conventional techniques for immobilizing enzymes on sensors surfaces encompass entrapment, encapsulation, crosslinking, covalent binding, and adsorption [125, 126]. Since the performance of biosensors heavily relies on the characteristics of the surface-confined architecture [127, 128], the choice of functionalization method must be made with utmost care to preserve the enzymatic activity and functionality of the transducing element. It should be noted that covalent attachment of biomolecules may not only damage the sp2 structure of graphene [129], but also potentially disrupt the folding and enzymatic activity if specific groups are involved in the immobilization [130].

In this regard, the use of LbL assembly has become very useful and remains an important strategy to integrate enzymatic assemblies on FET devices. Piccinini *et al* [131] employed the LbL assembly in combination with the intrinsic pH sensitivity of reduced graphene oxide (rGO) field-effect transistors (FETs) as a strategy to detect the enzymatic conversion of urea (figure 14). LbL assemblies were built up onto the sodium 1-pyrenesulfonate (SPS)-modified rGO FETs by alternate adsorption of cationic PEI and urease (negatively charged at physiological pH).

Figure 14(c) displays a representation of the drain-source current ( $I_{ds}$ ) plotted against the gate-source voltage ( $V_g$ , using an Ag/AgCl gate electrode), while maintaining a fixed source-drain potential ( $V_{ds}$ ), for a reduced graphene oxide (rGO) field-effect transistor (FET). By applying an external



**Figure 15.** (a) Change in the channel current ( $\Delta I_{ds}$ ) of a SPS/PEI-modified rGO FET monitored in real-time varying the pH from 5 to 10. (b)  $\Delta I_{ds}$  as a function of pH for a SPS-modified rGO FET (squares) and a SPS/PEI-modified rGO FET (circles). Experimental conditions: flow rate = 300  $\mu$ l min<sup>-1</sup>,  $V_g = -0.2$  V and  $V_{ds} = 0.1$  V. (a) Real-time monitoring of the change in channel current ( $\Delta I_{ds}$ ) of an SPS/PEI-modified rGO FET with variation in pH from 5 to 10. (b) Representation of  $\Delta I_{ds}$  versus pH for both an SPS-modified rGO FET (represented by squares) and an SPS/PEI-modified rGO FET (represented by circles). The experimental conditions for both plots include a flow rate of 300  $\mu$ l min<sup>-1</sup>, a gate voltage ( $V_g$ ) of -0.2 V, and a drain voltage ( $V_{ds}$ ) of 0.1 V. Solid lines are the linear regression fits. (c) Scheme of PEI as a reactive signal amplifier for pH changes. Reprinted from [131], Copyright (2017), with permission from Elsevier.

electric potential, the Fermi energy of the rGO can be shifted, leading to the modulation of the charge carrier density, which in turn causes a change in  $I_{ds}$ . The minimum  $I_{ds}$  (Dirac point, at  $V_g = V_i$ ) at pH 6 (figure 14(c)) is found at  $V_i = 95$  mV. At  $V_i$ , there is a transition between a regime with holes as charge carriers (for  $V_g < V_i$ ) and a regime with electrons as charge carriers (for  $V_g > V_i$ ). The charge carrier mobility ( $\mu$ ) of the device was found to be 30 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup> for holes and 15 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup> for electrons.

As mentioned earlier, the electrostatic LbL assembly method was employed for the non-covalent immobilization of the enzyme urease onto the channel of the reduced graphene oxide (rGO) field-effect transistors (FETs). Figure 14(d) illustrates the assembly process of the urease-PEI multilayer, denoted as  $(PEI/urease)_n$ , As this type of enzymatic sensor relies on the detection of small changes in pH caused by the hydrolysis of urea (figure 14(e)), the transfer characteristics of the transistors in a liquid-gated configuration under different pH values represent a critical aspect of the device. Figure 14(c) depicts the transfer characteristics of a SPSmodified reduced graphene oxide (rGO) FET measured at contact ionic strength under different pH conditions. It is observed that the slope of the transfer characteristics remains relatively unchanged for both sides V<sub>i</sub>. This observation implies that the charge mobilities of holes and electrons are independent of the pH. However, a noticeable shift of  $V_i$  to more positive  $V_{g}$  values was observed with increasing pH. Both,  $V_{\rm i}$  values and the change in the  $I_{\rm ds}$  ( $\Delta I_{\rm ds}$ ) showed a direct correlation with pH, wherein the change in pH resulted in a linear increase with a slope of  $23 \pm 1.8 \text{ mV pH}^{-1}$  and  $20.3 \pm 0.6 \,\mu\text{A pH}^{-1}$ , respectively.

Subsequently, an investigation was conducted on the impact of the PEI layer on the pH-response. The initial PEI layer exhibited a charge density of  $0.011 \text{ Cm}^{-2}$ , in agreement

with reported literature values for polyelectrolyte multilayers. The change in the registered  $I_{ds}$  of a rGO/SPS/PEI fieldeffect transistor while flowing solutions of increasing pH value are depicted in figure 15(a). It is observed that a pH change from 5 to 10 results in remarkable increase in  $I_{ds}$ . Furthermore, a detailed analysis reveals a linear relationship between  $I_{ds}$  ( $\Delta I_{ds}$ ) and the pH with a sensitivity (slope) of  $25.9 \pm 0.6 \,\mu\text{A pH}^{-1}$ . In figure 15(b),  $\Delta I_{\rm ds}$  is plotted against pH both prio to and after the PEI modification step. Transistors that underwent PEI modification demonstrated a 30% increase in pH sensitivity from 20.3 (prior to modification) to  $25.9 \,\mu\text{A pH}^{-1}$  (post modification). This observation can be explained by the characteristics of PEI, which is a weak polycation (pKa 8-9). Hence, as pH increases, the degree of protonation of the polymer decreases. This decrease in protonation leads to a change in charge density, which causes p-doping of the graphene layer via the 'electrostatic gating effect' (as illustrated in figure 13(c)). Polymer brushes of N,N-dimethylaminoethyl methacrylate groups on graphene-based FETs have also demonstrated similar behavior, as reported by Piccinini et al [132]. Hence, the weak polycation serves a two-fold role within the interfacial architecture: (i) as a building block for the LbL assembly, and (ii) as a transducer element to intensify the detection of local pH variations, thus acting as 'reactive signal amplifiers.'

The graph in figure 16(a) (top) displays the transfer characteristics of a system with and without 100  $\mu$ m urea, represented by solid and dashed lines, respectively. The presence of urea caused a clear shift towards more positive values of  $V_i$ , similar to the effect of increasing solution pH. This shift occurs due to enzymatic hydrolysis of urea, which generates NH<sup>4</sup><sub>4</sub>, HCO<sup>2</sup><sub>2</sub>, and OH<sup>-</sup> ions, as shown in figure 14(e). As a result of this pH change near the rGO, and



**Figure 16.** (a) (Top panel) Transfer characteristics of a (PEI/Urease)<sub>1</sub>-rGO FET under two conditions: in the absence of urea (blue trace) and in the presence of 100  $\mu$ m urea (red trace). (bottom panel) Change in the channel current upon switching from flow to batch (stagnant) measuring conditions. Real-time channel current response ( $\Delta I_{ds}$ ) upon exposure to different concentrations of urea for graphene transistors modified with (PEI/Urease)<sub>1</sub> (b) and (PEI/Urease)<sub>3</sub> assemblies. Reprinted from [131], Copyright (2017), with permission from Elsevier.

the accompanying alteration of the charge density of the PEI, the  $V_i$  shifts significantly towards a more positive gate voltage.

The bioelectronic response of transistors in the presence of a 100  $\mu$ m urea solution is shown in figure 16(a) (bottom) in real-time. The analyte solution was passed through the transistor for 4 min, allowing Ids to reach a plateau (flow response). Upon stopping the flow, there was an increase in Ids (static response), as can be seen in the graph.

Noteworthy, once the flow is resumed, the  $I_{ds}$  current value returns to the original value observed under flow conditions. This  $I_{ds}$  response can be explained in terms of mass transport phenomena taking place in the surroundings of the sensor surface. During flow conditions, hydroxyl ions that arise from the enzymatic process are rapidly removed from the surface of graphene due to forced convection. However, when the flow is stopped, the diffusion becomes the primary mechanism for the transport of hydroxyl ions away from the film, leading to an increase in their local concentration near the graphene surface. This results in significant electrostatic changes in the environment surrounding the graphene, which ultimately manifest as an increase in the recorded Ids, as a result of the enzymatic process. As shown in figure 16(b), an increase in urea concentration leads to an increase in Ids, in both flow and static conditions. However, when the urea concentration exceeds 1 mM, the enzyme can be inhibited by high substrate concentration, leading to the cessation of the enzymatic transduction mechanism.

By comparing the  $\Delta I_{ds}$  response as a function of logarithmic urea concentration for transistors modified with different numbers of enzyme-containing multilayers, we can observe the effect of the number of multilayers on the device sensitivity. This comparison is presented in figure 17.

It is observed that, by increasing the number of enzymepolyelectrolyte multilayers, it is possible to magnify the local effects arising from the enzymatic process with a concomitant effect on the transduced bioelectronics signal. The experimental results demonstrate that increasing the number of



**Figure 17.** The dependence of  $\Delta I_{ds}$  flow response (at a flow rate of 300  $\mu$ l min<sup>-1</sup>) on urea concentration was studied for (PEI/Urease)<sub>1</sub> (red), (PEI/Urease)<sub>2</sub> (blue), and (PEI/Urease)<sub>3</sub> (green) multilayers. The error bars depicted in the plot indicate the standard deviation obtained from measurements on three separate devices. Reprinted from [131], Copyright (2017), with permission from Elsevier.

bilayers from one to two and three respectively, results in a sensitivity increase of 20% and 68% compared to a single PEI/urease bilayer. This implies that greater local pH variations occur within the film as the number of bilayers increases. The approach of LbL assembly technique offers significant advantages in the production of enzyme-containing films with the ability to exert precise control over enzyme



**Figure 18.** Schematic of the LbL-assembled structure using PEI as the cationic building block, and urease and arginase as both recognition elements and anionic building blocks. The figure describes the reaction of the conversion of L-arginine into L-ornithine and the intermediate substrate urea by the enzyme arginase (EC 3.5.3.1) and the following urease (EC 3.5.1.5)-catalyzed hydrolysis of urea.

coverage on the surface of graphene. This technique can be seen as a valuable method for the creation of sensors displaying tailorable enzymatic activity as it offers the opportunity to tune the sensitivity and selectivity of interfacial architectures in a controllable manner.

Very recently, Fenoy *et al* employed the abovementioned strategy and extended it to the use of other polyamines, particularly PAH [82]. In this regard, the construction of PAH-urease (PAH-Urease)<sub>n</sub> assemblies not only allowed for the fabrication of urea graphene-based biosensors but also for the investigation of the effect of phosphate-amino interactions on the performance of the biosensing devices.

Interestingly, these notions can be further expanded to coupled enzymatic reactions [65], thereby broadening the spectrum of detectable analytes. Coupled enzymatic reactions or enzymatic cascade reactions refer to biomolecular systems in which a series of enzymes are coupled in such a way that the product of one enzyme is the substrate for the next.

In this section we will discuss the formation of enzymatic cascades combining arginase and urease with the aim of sensing L-arginine using gFETs as transducers. L-arginine, an amino acid used in the biosynthesis of proteins, plays a vital role in various biological functions of living organisms, including the cardiovascular, immune, and endocrine systems [133]. Monitoring the levels of L-arginine in physiological fluids is therefore of significant interest in clinical diagnostics.

The development of the L-arginine sensor involved the immobilization of arginase and urease on the reduced graphene oxide surface through a LbL assembly process (figure 18) [134]. The enzymatic cascade process involves two reaction steps, where arginase hydrolyzes L-arginine in the first step, yielding ornithine and urea, which do not trigger any sensor response. In the second step, urea acts as a substrate and is converted by urease into NH<sub>3</sub> and CO<sub>2</sub>,

leading to an increase in pH levels in the immediate surroundings of the rGO-FET surface (as illustrated in figure 18). This increase in pH can be detected by the graphenebased field-effect transistors, thereby indicating the presence of L-arginine.

Enzyme immobilization through electrostatic LbL assembly using PEI as polycation represents a critical step in the sensor construction. As already discussed, weak polycations play a key role as 'reactive signal amplifiers'. Enzymatic cascades require precise control of the enzyme spacing and loading within the assembly, as well as optimization of the enzyme ratio. In such scenarios, PEI plays a critical role, enabling the fine-tuning of these parameters to achieve optimal sensor performance. This structural role of PEI is of great importance in the transduction of the multistep cascade reaction taking place on the graphene surface.

The sensing approach based on the enzymatic cascade involves the coupling of both arginase and urease enzymes to produce a pH increase in the presence of L-arginine. At negative gate voltage ( $V_g$ ), the accumulation of OH<sup>-</sup> in the vicinity of the rGO-FET surface results in an increase in the hole carrier concentration, which can be measured as an increase in the source-drain current ( $I_{ds}$ ) (as shown in figures 19(a) and (b)).

The multilayer architecture containing both arginase and urease enzymes plays a critical role in the sensing performance. The close proximity of these enzymes is essential for optimal catalytic conversion of the analyte, which is achieved through a cascade reaction [135]. Figure 19(c) describes the response of graphene transistors modified with different configurations of urease and arginase assemblies in the presence of different concentrations of L-arginine (figure 19(d)). Urease and arginase were coimmobilized in the outermost layer of these structures. To



**Figure 19.** (a) Real-time channel current response ( $\Delta I_{ds}$ ) for the PEI-Ur-PEI-UrAr-PEI assemblies displaying different enzyme ratios in the outermost layer: (a) Ur:Ar = 1:1 (b) Ur:Ar = 1:2. (c)  $\Delta I_{ds}$  response of the assemblies PEI-UrAr-PEI Ur:Ar 1:1 (R = 0.90) (red circles), PEI-Ur-PEI-UrAr-PEI Ur:Ar 1:1 (R = 0.99) (blue circles) and PEI-Ur-PEI-UrAr-PEI Ur:Ar 1:2 (R = 0.99) (green circles). Linear regression fits are also represented in the plot. (d) Cartoons depicting the different bienzymatic arrays assembled on the transistor. Reproduced from [134]. CC BY 4.0.

enhance the pH-shifting enzymatic conversion in proximity to the graphene surface, additional urease was incorporated in the bottom layer of the assembly.

The experimental data reveal that PEI-Ur-PEI-UrAr-PEI (Ur:Ar 1:2) assemblies exhibit the best performance in comparison with PEI-Ur-PEI-UrAr-PEI (Ur:Ar 1:1) and PEI-UrAr-PEI. Therefore, it is the ratio between both enzymes in the bi-enzymatic cascade reaction has a relevant effect on the sensor performance. Assemblies exhibiting a Ur: Ar 1:2 ratio in the outermost enzyme layer of the assembly undergo a more extensive analyte conversion leading to higher intermediate substrate (urea) concentrations. Using an excess of urease ensures the rapid conversion of all intermediate species, making the observed rate of ammonia formation directly proportional to the concentration of arginine. The optimization of the interfacial architecture involving an increase in the Ur:Ar ratio from 1:1 to 1:2 resulted in a sensitivity increase from 24 to 33.5  $\mu$ A per decade [L-arginine] in the 10–1000  $\mu$ m concentration range.

Enzymatic interfacial architectures have also been integrated on ion-sensitive FETs (ISFETs) through LbL assembly in order to detect acetylcholine. Similarly to the signal transduction mechanism of urea sensors, the enzymecatalyzed hydrolysis of acetylcholine generates a change in the pH which is detected by the ISFET [136]. In this regard, Liu *et al* [137] proposed the construction of acetylcholinesensitive ISFETs through the LbL assembly polymer/ nanoparticle composites integrating polyaniline (PANI) as the semiconductor channel material. Figure 20 illustrates the schematic layout of an enzymatic ISFET that is sensitive to acetylcholine. Its structure closely resembles that of a standard thin-film transistor, with one key exception: the gate electrode has been replaced with a reference electrode made of silver/silver chloride (Ag/AgCl).

Five layers of PANI were assembled on the substrate in the sequence of  $[PANI + PSS]_5$ . Next, the SiO<sub>2</sub> nanoparticles were integrated in the sequence of  $[PDDA + SiO_2]_6$ . Then, acetylcholinesterase (AChE) was assembled on the top surface of SiO<sub>2</sub> nanoparticle thin film. In this configuration, PANI multilayers play their role as the channel, the selfassembled SiO<sub>2</sub> nanoparticles act as the gate dielectrics and acetylcholine esterase operates as the biorecognition element. To facilitate the assembly of the different components, three bilayers of PDDA/PSS were used as priming layers in



**Figure 20.** (Left) Schematic diagram of the acetylcholine sensitive ion-sensitive field-effect transistor. (Right) Hydrolysis reaction of acetylcholine to form acetate ion and choline resulting from the catalysis of acetylcholinesterase. Reprinted from [137], Copyright (2007), with permission from Elsevier.



**Figure 21.** (a) Variation in the drain current ( $I_d$ ) as a function of the acetylcholine concentration for an AChE-modified PANI ISFET. (b) Time-resolved gate voltage response for an AChE-modified PANI ISFET exposed to solutions with increasing acetylcholine concentration: (A) DI water, (B) 10 nm, (C) 100 nm, (D) 1  $\mu$ m, (E) 10  $\mu$ m, (F) 100  $\mu$ m, (G) 1 mm, and (H) 10 mm. Reprinted from [137], Copyright (2007), with permission from Elsevier.

building the structure. The substrate was then coated with five PANI/PSS bilayers, i.e.: [PANI + PSS]<sub>5</sub>. Following this, six layers of SiO<sub>2</sub> nanoparticles were assembled in combination with PDDA, [PDDA + SiO<sub>2</sub>]<sub>6</sub>. Finally, acetylcholinesterase (AChE) was integrated onto the device via direct adsorption/ assembly on the SiO<sub>2</sub> nanoparticle thin film. The PANI multilayers, SiO<sub>2</sub> nanoparticles, and acetylcholine esterase each serve a specific role in the structure. The PANI multilayers function as the channel material, while the self-assembled SiO<sub>2</sub> nanoparticles act as the gate dielectrics. Finally, the AChE operates as the biorecognition element within the system. As mentioned earlier, the LbL-assembled acetylcholine ISFET biosensor operates on the principle of enzymatic hydrolysis of acetylcholine in the presence of

AChE, as depicted in figure 20. This hydrolysis reaction generates acetic acid, which reduces the pH of the surrounding solution, leading to local electrostatic changes that can be detected by the ISFET. It is important to note that ISFETs are especially effective at detecting slight pH changes [138, 139].

The sensitivity of a LbL-assembled PANI ISFET for different acetylcholine concentrations is shown in figure 21(a). At low acetylcholine concentrations, the drain current is also small due to the low proton concentration generated during the reaction between acetylcholine and AChE. However, it is clear that the LbL-fabricated ISFET is sensitive to the presence of acetylcholine and can detect a concentration change of the analyte down to  $1 \mu m$ . The response time of the LbL-assembled PANI ISFET to changes in the open circuit potential for varying concentrations of acetylcholine is depicted in figure 21(b). As the concentration of acetylcholine in the solution increases, the voltage between the drain electrode and Ag/AgCl reference electrode also increases. These findings demonstrate that the LbL-assembled device delivers excellent sensing performance, operating at very low voltages while maintaining high mobility.

Summarizing, we have described, in the previous examples, the use of LbL-assembled enzymatic FETs, in which enzymatic reactions alter the electrostatic conditions in the surroundings of the channel or gate interfaces, producing an electronic signal dependent on the concentration of a particular analyte.

On the other hand, the use and application of nanoparticles in biosensor design has gained increasing attention in bioanalytical chemistry due to their unique properties. Studies indicate that  $MnO_2$  nanoparticles can react with hydrogen peroxide to form  $Mn^{2+}$  and  $O_2$ , while using up two hydrogen ions. This means that  $MnO_2$  nanoparticles work as an oxidizing agent, reacting with  $H_2O_2$  (in contrast to the properties exhibited by bulk  $MnO_2$ ), and ultimately leading to an increase in pH. Consequently, this presents an opportunity to establish a biosensing system that performs multiple functions, whereby changes in pH caused by the catalytic reaction can be detected by the transistor.

Xu and colleagues [140] employed this idea to create biosensors that rely on oxidase-based FETs, where minimal pH changes occurred during the enzymatic reaction. They accomplished this by combining lactate oxidase (LOD) and  $MnO_2$  nanoparticles into PDDA films through a LbL selfassembly technique to generate (PDDA/MnO<sub>2</sub>/PDDA/LOD)<sub>n</sub> multilayers on the FETs. To achieve a highly charged surface that can stably absorb the LOD layers, the substrates were modified beforehand using a PSS/PDDA priming layer. By layering PDDA, nanoparticles, PDDA, and enzyme sequentially up to six times, PDDA/MnO<sub>2</sub>/PDDA/LOD multilayers were incorporated onto the FET devices (as illustrated in figure 22(a)).

The FETs modified with (PDDA/MnO<sub>2</sub>/PDDA/LOD)<sub>3</sub> (depicted in curve a in figure 22(b)) exhibit a response, where the open circuit potential shifts to more negative values when lactate is introduced due to the decrease in H<sup>+</sup> concentration near the sensitive gate surface. The response time of these FETs is under 100 s. Control experiments using enzyme-free  $(PDDA/LOD)_n$  modified FET revealed that in the presence of lactate only a small response is observed. The calibration curves of LbL-assembled FETs with and without MnO2 nanoparticles are shown in the inset of figure 22(B). The device sensitivity is  $\sim 0.34 \text{ mV mm}^{-1}$ without MnO<sub>2</sub> nanoparticles, as shown in curve b. Conversely, when multilayers containing MnO2 nanoparticles are present, the sensitivity of the ENFET increases to  $16.84 \text{ mV mm}^{-1}$ . Hence, the use of nanocomposite multilayers incorporating MnO<sub>2</sub> nanoparticles promotes a 50-fold increase in sensitivity. These nanocomposite LbL devices exhibited an extended dynamic range up to 6.0 mm displaying a linear range between  $1.0 \times 10^{-5}$  and  $3.6 \times 10^{-3}$  M, with a detection limit of 8  $\mu$ m.



**Figure 22.** (A) Schematic diagram of multilayer films, consisting of lactate oxidase and  $MnO_2$  nanoparticles, assembled on a FET. (B) Response of FET devices modified with multilayer assemblies to the presence of lactate. Plots correspond to films with (a) and without (b)  $MnO_2$  nanoparticles. The calibration curve of the FET, with (a) and without (b)  $MnO_2$  nanoparticles, is shown in the inset. Reproduced from [140] with permission from the Royal Society of Chemistry.

### 4.2. LbL assembly as a strategy to increase the interfacial sensitivity of field-effect transistors

The development of graphene sensors has represented the advent of new platforms for the rapid detection of chemical and biological species with a high degree of sensitivity. However, it is known that the response of these types of devices is affected by the screening of mobile ions in the vicinity of the graphene surface, and for this reason, performing measurements in saline environments similar to physiological ones is not a simple task. These sensors are sensitive to the electrostatic potential generated in the vicinity of graphene by the presence of charged biomolecules [141]. Nevertheless, the presence of mobile ions screens these electrostatic effects caused by the analyte, reducing the sensitivity of the interfacial region to a length scale given by the Debye length ( $\kappa^{-1}$ ). Within this length scale, surface charges are neutralized by mobile ions from the electrolyte. In the case where  $\kappa^{-1}$  is smaller than the distance between the



**Figure 23.** (a) Transfer characteristics of graphene FETs modified with PDDA/PSS multilayers (first bilayer: solid line; second bilayer: dashed line; PDDA-terminated assemblies: blue trace; PSS-terminated assemblies: red trace). The left and right panel depict the assemblies prepared under low and high conditions, respectively. (b) Variation in the Dirac point ( $\Delta V_i$ ) as a function of the number of layers assembled on the graphene transistor. Symbols colored in orange and green correspond to polyelectrolyte multilayers prepared under low and high ionic strength conditions, respectively. (c) Schematic representation of the polyelectrolyte multilayer prepared from PDDA and PSS, with overcompensation of charges at the outermost layer. The figure also displays a representation of the potential,  $\psi(x)$ , versus distance, *x*, for a 1 mm KCl solution and a polyelectrolyte multilayer (d) Variation in the Dirac point,  $\Delta V_i$ , as a function of the number of layers assembled on the graphene transistor under high ionic strength conditions and measured in the presence 1 mM (green) and 10 mm KCl (red). The dashed lines indicate the condition in which the film thickness equals  $\kappa_p^{-1}$ . Reprinted with permission from [143]. Copyright (2018) American Chemical Society.

captured analyte and the graphene surface, the recognition process will not be properly detected by the sensor. FET sensors based on nanomaterials are an appealing platform for detecting chemical and biological species with high sensitivity, real-time monitoring, without requiring labeling protocols. However, their response is affected by the presence of mobile ions, and as a result, it is challenging to use them for sensing in solutions with physiological ionic strength. Under salt conditions similar to physiological ones, the strong electrostatic screening leads to a significant decrease of the characteristic length scale (<1 nm) where graphene transistors are sensitive to the presence of the analyte [142]. In fact, this value is much smaller than the size of many biomedical analytes of interest, such as proteins. Additionally, the size of the interfacial architecture that anchors the receptor further limits the distance between the analyte and the sensor surface. This mismatch between the size of the analyte and the characteristic length associated with the sensitivity region of the graphene transistor limits the use and application of this technique in clinical samples.

Piccinini *et al* [143] employed polyelectrolyte multilayers to extend the Debye length within the film, which helped to expand the sensitivity range of graphene transistors. They estimated the electrostatic screening length by measuring the thickness of the film and the potential drop across it. Figure 23(a) shows how the transfer characteristics of graphene transistors were modified with PDDA/PSS bilayers. The addition of PDDA, a cationic polyelectrolyte, shifted the Dirac point ( $V_i$ ) towards more negative values.

On the other hand, when the negatively charged PSS layer was added, it caused a shift in  $V_i$  to a more positive gate voltage. Experiments reported by Wang and Burke [144] demonstrated that the adsorption of macromolecules with either positive or negative charges induces a corresponding positive or negative charge on graphene. As a result, the Fermi energy shifts to the conduction or valence band, which explains this effect.

In the first ten layers,  $V_i$  was able to reverse after the addition of each layer. The data suggests that higher  $V_i$  shifts occurred when polyelectrolytes were assembled at high ionic strength. This is because the adsorption of polyelectrolytes at high ionic strength resulted in thicker layers and a higher surface charge density ( $\sigma$ ). The induced charges on graphene depend on the surface charge density, and an increase in charge density leads to larger  $\Delta V_i$ . Conversely, for multilayers prepared at low ionic strength (orange circles),  $V_i$ 



**Figure 24.** (A) LbL assembly process on organic electrochemical transistors (OECTs) (B) Transfer characteristics an organic electrochemical transistor modified with various polyelectrolyte layers. (C) Dynamic response of  $I_{DS}$  (drain-source current) of an OECT device during the consecutive assembly of polyelectrolyte layers. (D) Relative change in  $I_{DS}$  upon exposure of an OECT device different polyelectrolyte solutions. Polyelectrolyte concentration: 0.1 mg ml<sup>-1</sup>, supporting electrolyte: 0.1 M KCl. Operating conditions:  $V_{DS}$  –0.1 V, electrolyte: 0.1 M KCl. Reprinted with permission from [148]. Copyright (2022) American Chemical Society.

reversed after each layer. However, the assemblies made at 0.5 M KCl (green circles) showed a decrease in the absolute Vi shifts after the 12th layer, resulting in a damping effect (shown in figure 23(b)). From the 12th layer onward, there was a continuous decrease in  $\Delta V_i$  until the 20th layer, after which the Dirac point did not show a significant change.

As a result of the polyelectrolyte assembly process graphene transistors exhibit a shift in the Dirac point, which is attributed to the electrostatic properties of the multilayers. The Debye length inside the film  $(\kappa_p^{-1})$  differs from that in the solution  $(\kappa_s^{-1})$ , and this is clearly shown in figure 23(c). The shift is caused by an unbalanced charge overcompensation that is not counterbalanced by mobile ions. The surface potential and  $V_i$  changes are affected by not only the charge density of the top layer but also the electrostatic screening of mobile charges within the multilayer films [145]. Figure 23(d) indicates how  $\Delta V_i$  changes with the number of layers for films formed at high ionic strength and measured at 1 mm (green) and 10 mm KCl (red). The number of layers can be used to determine the thickness of the film, and the correlation between the thickness and  $\Delta V_i$  provides an estimate of the  $\kappa_p^{-1}$  value. These measurements helped estimate the concentration of mobile ions present within the polyelectrolyte multilayer: 0.006 and 0.073 mm for 1 and 10 mm KCl solutions, respectively. The Debye length inside the film at pH = 7 was also estimated for different salt concentrations, which were found to be 118.4, 37.4 and 9.6 nm for 1, 10 and 140 mm KCl. According to a thermodynamic model, this phenomenon can be attributed to the entropic cost involved in the confinement of ions within the polymer film. The electrostatic screening within the multilayer film is influenced by the density of the polymer and the concentration of ions in the solution. These experiments demonstrate that the use of PDDA/PSS multilayer films can significantly broaden the sensing range in physiological samples, increasing it from 0.82 to 9.6 nm. This LbL approach can be used to expand the sensing capabilities of FETs to a wide range of biomacromolecules including proteins and nucleic acids, making it highly relevant for biosensing in clinical settings.

The enhancement of the interfacial sensitivity by the engineering of the semiconducting surface with polyelectrolyte multilayers was also observed for graphene-FETs modified with mesoporous thin films and organic electrochemical transistors (OECTs) [146-148]. OECTs are a new type of field-effect transistors that use an organic semiconducting channel to connect the source and drain electrodes. The conductivity of this channel is controlled by a gate voltage applied through an electrolyte [149, 150]. These devices operate as a combination of ionic and electronic conductors, where the injection of ions from the electrolyte into the organic film is required to maintain a balanced charge [151-153]. Within this framework, Fenoy and co-workers fabricated OECTs using PEDOT-PAH, and used these devices to track the adsorption of polyelectrolyte multilayers (figure 24). By using the thermodynamic model, an effective Debye length inside the film of 9 nm was obtained, while the solution used for the measurements was a 0.1 M KCl with an estimated Debye length of 0.96 nm. Recently, Scotto and colleagues demonstrated that the gFET technology can be used to track the adsorption of both positive (PDDA) and negative (PSS) polyelectrolytes in realtime [154]. They employed a portable setup consisting of graphene-based field-effect transistors (gFETs). They performed a comparative kinetic analysis of the surface plasmon resonance (SPR) and gFET responses to correlate the gFET response with mass adsorption processes. Figure 25 presents the comparison of the  $\Delta \theta$  curves of SPR signal (black squares) with the gFET signal (green circles) during the adsorption of PDDA. Remarkably, both techniques showed the same kinetic behavior, even when the adsorption took



**Figure 25.** Comparison of the kinetic  $\triangle$ SPR curves (black circles) with the gFET signal (green circles) for the adsorption of PDDA. Reprinted with permission from [154]. Copyright (2022) American Chemical Society.

place at considerable distances from the sensing surface. The authors showed that under specific conditions, the electronic response is directly linked to mass adsorption. Therefore, gFETs can be used to investigate the interaction of charged macromolecules, enabling the determination of kinetic profiles and critical binding parameters.

#### 5. Conclusions

In modern technology, FETs have been the most important electronic devices, and represent the basic building blocks of the systems of modern information, communication and (bio)sensing technologies. The progress in these important fields critically depends on rapid improvements of FET performance. Although silicon is the dominant semiconducting material, two-dimensional materials and conducting polymer thin films have been demonstrated tremendous potential for the fabrication of FET devices for electronic and bioelectronics applications [155, 156]. Transistors with precise and rational nanoarchitecture of the semiconducting materials, dielectrics and functional (bio)components are required. In this review article, we describe how the convergence between the semiconducting nanomaterials and the LbL nanoarchitectonics allows generating integrated systems for FET device configurations with extraordinary properties and functions.

Research efforts to engineer FETs using the solutionbased LbL assembly approach are exemplified according to classification of semiconducting materials, dielectrics, and how the LbL technique can be used to incorporate (bio) functionalities to the device. This nanoadditive manufacturing strategy guarantees the precise control over the construction of the different elemental components of the transistor (i.e. channel, dielectric, and electrodes). With this technique, for instance, semiconducting channels are prepared by the deposition of different materials such as carbon nanotubes, graphene, graphene oxide, conducting polymers and transition-metal dichalcogenides. Interestingly, the LbL technique presents self-limiting nanoadditive features what simplify the nanoengineering of the FETs devices. In this regard, several protocols for the fabrication of SWCNT-FETs, graphene-FETs, and heterostructured two-dimensional-FETs were described and discussed.

The LbL technique can be used also to manipulate gate dielectrics to control the capacitance, mobility, hysteresis, and other critical device parameters in electronics. For instance, the LbL construction of  $[PEI/2D \text{ montmorillonite}]_n$  and  $[PEI/hexagonal boron nitride]_n$  films can act as effective dielectrics with leakage currents below  $10^{-8} \,\mathrm{A}\,\mathrm{cm}^{-2}$  and  $3 \times 10^{-9} \,\mathrm{A \, cm^{-2}}$ , respectively. These dielectric films enable low voltage operation, with negligible hysteresis and high mobilities. Furthermore, oppositely charged polyurethanes can be self-assembled to build 15 nm thick elastomeric nanodielectrics leading to the fabrication of soft and hysteresis-free FETs. Compared with atomic layer deposition or chemical vapor deposition, solution-based LbL assembly offers a more economical and scalable strategy to create tailored films. Furthermore, the LbL approach also offers advantages over spin coating in controlling thickness in the ultrathin limit.

Nanoachitectonics cannot only be used for the construction of the elemental components of the transistor but also for the semiconductor surface engineering to confer (bio) functionality. By integrating biorecognition elements, such as enzymes that are embedded in LbL assemblies on the semiconducting surface, it is possible to create biosensors that are highly sensitive, label-free, and capable of real-time monitoring. Enzymes are ideal recognition elements for this purpose because of their selectivity and specificity towards the analyte. For example, the electrostatic LbL assembly of the enzyme urease and the polycation PEI onto the channel of the rGO FETs results in real-time urea biosensors. This functional biosensor system takes advantage of both the pH sensitivity of graphene-based transistors and the alteration in local pH resulting from the catalyzed hydrolysis of urea. Interestingly, the transistors modified with  $(PEI/urease)_n$ resulted in an increase in pH sensitivity since the weak polycation act as a transducer element to amplify the detection of local pH changes, i.e.: 'reactive signal amplifiers'. In this case, the convergence between LbL nanoarchitecture and FET transduction capacity results in devices that are able to real-time urea monitor with a limit of detection (LOD) down to 1 µM, fast response and good longterm stability. Other enzymes such as acetylcholine esterase and lactate oxidase were also incorporated on FET devices using the LbL technique for real-time detection of acetylcholine and lactate, respectively.

This approach can be further extended to coupled enzymatic reactions, thereby broadening the spectrum of detectable analytes. In this sense, nanoarchitectured integrated systems of more than one enzyme can be designed on FETs for enzymatic cascade biosensing. For example, combining arginase and urease in the LbL nanoarchitecture on the graphene surface, FET biosensors for L-arginine can be fabricated. In the case of enzymatic cascades, PEI plays a crucial role as it allows for precise tuning of the enzyme spacing and loading within the assembly what is of great importance in the transduction of the multistep cascade reaction taking place on the graphene surface.

The nanoengineering of the FET surface can lead to a great enhancement of the interfacial sensing. LbL assembled films made of PDDA/PSS polyelectrolytes are capable to abruptly increase the sensing range of both graphene and organic FETs. The Debye length within the multilayer film increases by more than one order of magnitude, as observed in a set of experiments. According to a developed thermodynamic model, this is primarily due to the entropic expense of confining ions within the polymer film. Multilayer films are highly significant for (bio)sensing in physiological samples, as they can extend the sensing range from 0.82 to 9.6 nm. By using the LbL assembly of polyelectrolytes, the possibilities of FET sensing can be expanded from small molecules to a wide range of biomacromolecules, including proteins and nucleic acids.

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#### Data availability statement

The data cannot be made publicly available upon publication because they are not available in a format that is sufficiently accessible or reusable by other researchers. The data that support the findings of this study are available upon reasonable request from the authors.

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